

125KW PCS solution in high power density GWQ package

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Abstract

This paper introduces a new high power density package called GWQ. GWQ is the largest package for PCS applications. The test proves that the package will not deform in long-term use. The module uses the new M7I chip technology with the NPC-T topology. A single module can meet the power output of 125KW PCS. At the same time, it is obtained by simulation that the Sic MOSFET or Sic SBD mixed with IGBT can reduce the system loss by 15%~32% and increase the efficiency by 0.22%~0.55%. The Tjmax of the chip is reduced by 4~7°C through thermal simulation. Through the test data, the GWQ module scheme has excellent effect in 125KW PCS.

1 Introduction of 125KW PCS

The power of the energy storage PCS changes with the energy of the battery cell, and the most widely used PCS models are 100KW models. However, as the battery energy is upgraded from 280Ah to 320Ah, the power of PCS needs to be increased. Therefore, 125KW PCS will become the mainstream in the future.

2 GWQ package solution in 125KW PCS

This chapter describes the module solution applied in 125KW PCS, including topology, chip, package and other information. Through the using of GWQ packaging modules, customers can reduce the size and weight of 125KW PCS and reduce the risk of application failure.

2.1 Topology Scheme

The 125KW GWQ package uses NPC-T topology scheme. The topology is shown in Fig.1.

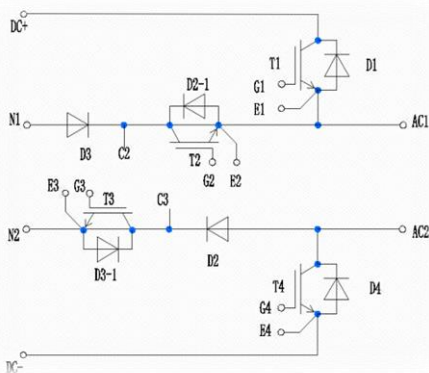


Fig.1 NPC-T topology

Compared with NPC-I converter circuits, the topology is simple and all of them are short converter circuits

with low Ls and voltage stress. The NPC-I topology is shown in Fig. 2.

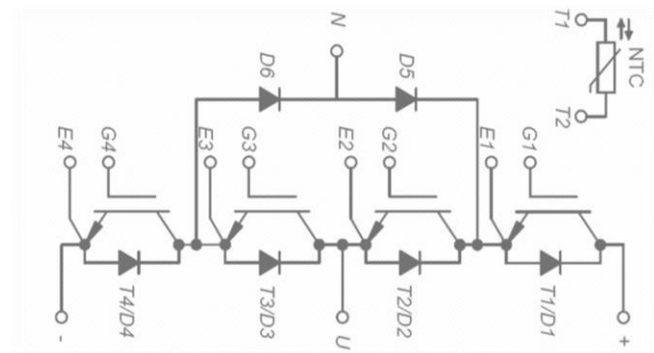


Fig.2 NPC-I topology

Due to the development of M7I 1200V devices, NPC-T standpipe has a suitable selection scheme, so the simple control of NPC-T can be used in high-power commercial and industrial PCS.

Compared with the previous scheme, the power loss can be reduced, and the switching frequency can be increased. At the same time, the application of M7I chip, NPC-T topology can have more advantages in loss than NPC-I.

The loss difference between the two topologies can be compared by simulation data. The loss data are shown in Table 1.

Table 1 Loss simulation data

1-a Simulation condition

Condition		
Parameter	Number	Unit
Vac	400	V
Vdc	950	V
Iout	190	A
Fsw	16	KHz
f	50	Hz
PF	1	

1-b Inverter simulation result

Parameter	Inverter			
	NPC-I		NPC-T	
Parameter	Number	Unit	Number	Unit
T1/T4 Ptot	120.48	W	148.42	W
T2/T3 Ptot	105.98	W	57.52	W
D1/D4 Ptot	0	W	0	W
D2/D3 Ptot	0	W	87.45	W
D5/D6 Ptot	88.7	W	/	W
Module Ptot	630.32	W	586.78	W

From the table, NPC-T topology is obviously more advantageous. Compared with NPC-I scheme, the discharge loss is reduced by 7%.

2.2 Chip scheme

The 125KW GWQ package uses M7I chip technology. The high-speed IGBT G7U 140A 1200V and the matching ultra-fast 140A 1200V FRD are used as the NPC-T standpipe. The high speed IGBT G7U 200A 750V and 200A 750V FRD are transverse tubes. Detailed configuration of the chip is shown in **Table 2**.

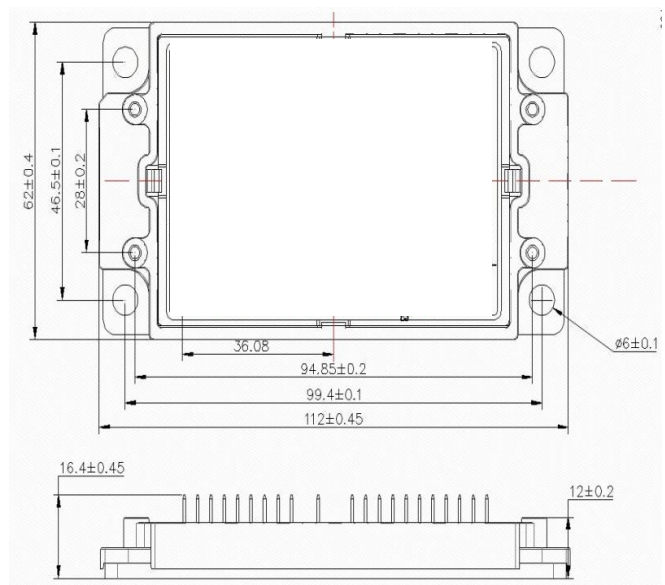
Table 2 Chip detail configuration

Unit	Number	Specification	Technology
T1/T4	3	140A 1200V	M7U
T2/T3	2	200A 750V	M7U
D1/D4	3	140A 1200V	M7D
D2/D3	2	200A 750V	M7D
D2-1/D3-1	1	75A 1200V	M5D+

The module applies the latest chip technology to make the $V_{ce(sat)}$ to a very low level, while ensuring that the IGBT reaches the high-speed switching of ns class. The application of this high-speed chip greatly reduces the loss in the application of bidirectional converter of energy storage, while ensuring that the voltage stress meets the application requirements.

2.3 Package reliability

The GWQ package is 62mm wide, 112mm long and 12mm high, with a copper base plate. **Fig. 3 (a)** shows the size of the GWQ package. **Fig. 3 (b)** shows the GWQ package 3D diagram.

**Fig.3 (a)** The size of the GWQ package

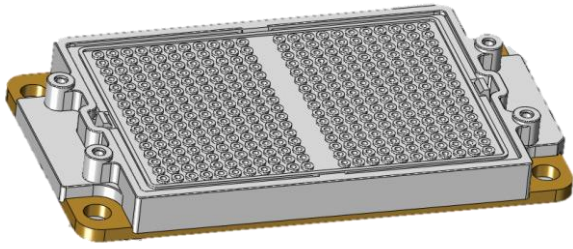


Fig.3 (b) The GWQ package 3D diagram

GWQ compared to similar size package without copper base plate, long-term use will not have the risk of shell deformation. Lock the copper base plate and bare DBC product onto the radiator for temperature cycle. The results are shown in **Table 3**.

Table 3 Comparison of TC life of modules with and without baseplate

No.	Yes/No BP	Number	Cycle to failure
1	Yes	6	2000
2	No	6	600
3	Yes	6	1800
4	No	6	700

As can be seen from table, the service life of a module with a copper baseplate is higher than that of a bare DBC module.

Through the special treatment of module DBC and the upgrade of silicon gel, HV-H2S and salt spray tests can also be passed using GWQ packaging.

3 Advantages of the third-generation semiconductor used in GWQ

3.1 Hybrid module of SIC SBD

Since the energy storage application is a two-way power conversion, all FRDS of NPC-T need to be replaced by SiC SBD.

Table 4 shows the chip configuration after the SIC SBD is replaced.

Table 4 The chip scheme after mixing SIC SBD

Unit	Number	Specification	Technology
T1/T4	3	140A 1200V	M7U
T2/T3	2	200A 750V	M7U
D1/D4	5	50A 1200V	/
D2/D3	5	50A 1200V	/
D2-1/D3-1	1	75A 1200V	M5D+

Through simulation, the current discharge, pure reactive power and charging loss of 125KW PCS before and after using SIC SBD were compared.

The results showed that the loss of using FRD was about 18%~46% higher than that of SIC SBD in each working condition. The simulation results are shown in the **Fig 4**.

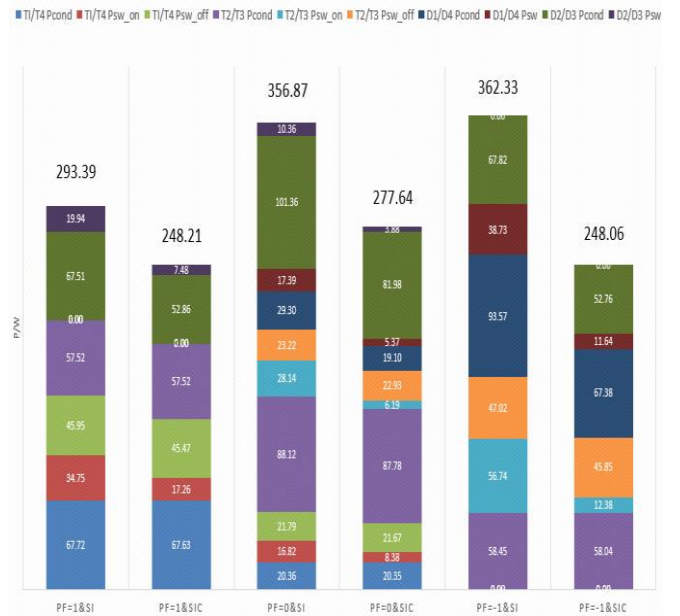


Fig 4 Power loss comparison between SIC SBD scheme and SI scheme

If only the power device loss is considered, the efficiency of the whole machine can be increased by about 0.22%~0.55%.

3.2 Hybrid module of SiC MOSFET

Sic MOSFET only needs to replace the IGBT of the standpipe, and the switching characteristics of the standpipe are optimized.

Due to the presence of the Sic MOSFET's body diode, Eon of the transverse tube are also optimized.

Table 5 shows the chip configuration after the SIC MOSFET is replaced.

Table 5 The chip scheme after mixing SIC MOSFET

Unit	Number	Specification	Technology
T1/T4	4	14.4mΩ 1200V	/
T2/T3	2	200A 750V	M7U
D1/D4		Body diode	/
D2/D3	2	200A 750V	M7D
D2-1/D3-1	1	75A 1200V	M5D+

Through simulation, the discharge, pure reactive power and charging loss of 125KW PCS before and after using SIC MOSFET were compared.

The results showed that the loss of IGBT was about 22%~35% higher than that of SIC MOS under each working condition.

The simulation results are shown in the **Fig 5**.

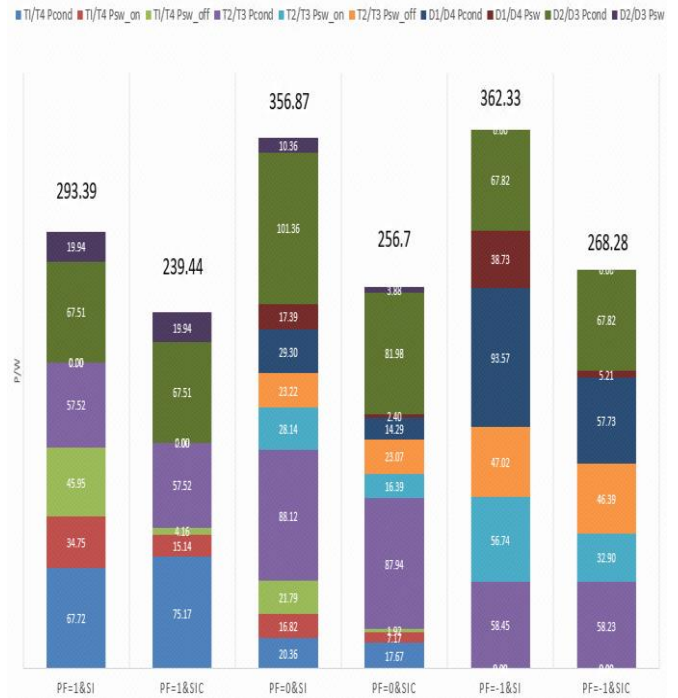


Fig 5 Power loss comparison between SIC MOSFET scheme and SI scheme

If only the power device loss is considered, the efficiency of the whole machine can be increased by about 0.26%~0.45%.

3.3 Advantages of third-generation semiconductors

Through the above third-generation semiconductor and SI material device loss comparison, the SIC device has excellent device characteristics.

Here are some of the advantages of third-generation semiconductors.

1. The material has wider band gap and stronger pressure resistance.
2. With higher energy density, the chip area of the same power can be reduced.
3. High thermal conductivity, high temperature resistance, high reliability, chip area can be reduced.

4 Experimental verification of 125KW PCS

Through the load test of 125KW PCS, the Si solution of GWQ package meets the application. The whole machine test diagram is shown in Fig.6.

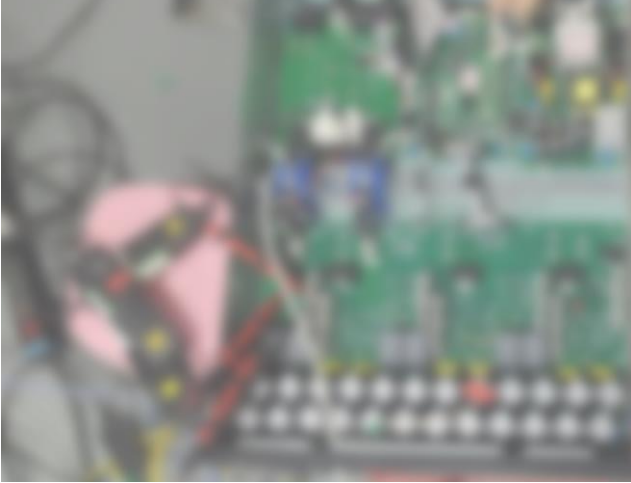


Fig.6 125KW PCS load test

The SIC hybrid scheme is consistent with the simulation data, and the system loss of the whole machine is reduced by 15%~32% compared with the pure Si scheme. The efficiency is increased by 0.22%~0.55%.

By embedding thermocouple wire, the thermocouple wire reading is monitored during the whole machine test. See Fig.7 for thermocouple test.



Fig.7 SIC hybrid scheme thermocouple test

According to the test results, the maximum junction temperature of T1 is 76.3°C, which is 9°C lower than that of all-silicon scheme.

5 Conclusion

This paper introduces the application of GWQ package for 125KW PCS, and introduces a new high-density package GWQ from the aspects of chip selection, topology selection and package reliability.

At the same time, the mixed sealing of the third-generation semiconductor makes a great contribution to the efficiency improvement. Compared with the Si scheme, the system loss of the whole machine is reduced by 15%~32%, the efficiency is increased by 0.22%~0.55%. The T_{jmax} of the chip is reduced by 9°C.

In summary, the high-power density GWQ package has a great competitive advantage in 125KW PCS applications.

6 References

- [1] D. Xu, H. Lu, L. Huang, S. Azuma, M. Kimata and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices", IEEE Transactions on Industry Application, vol. 38, no. 5, pp. 1426-1431, Oct. 2002.
- [2] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," in Proceedings of the IEEE, vol. 90, no. 6, pp. 969-986, June 2002.